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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,925	07/07/2003	Takahiro Kawano	239801US2	6929
22850	7590	04/13/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/612,925

Applicant(s)

KAWANO ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 February 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) 2,3,7-20 and 25-38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-6,21-24 and 39-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Drawings***

The drawings were received on 02/03/2005. These drawings are approved by the examiner.

### ***Claim Objections***

Claims 1, 4-6, 21-24 and 39-41 are objected to because of the following informalities: The claimed limitation of "main electrodes and upper surfaces of the main electrodes", as recited in claims 1, 6 and 24, should read "main electrodes, and upper surfaces of the main electrodes".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4-6, 21-24 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narazaki et al. (6,285,058) in view of Applicant Admitted Prior Art (AAPA).

Narazaki et al. teach in figure 1 and related text a semiconductor device comprising:

a semiconductor layer which includes a first semiconductor region 2 of a first conductivity type, a base region 3 of a second conductivity type, and a plurality of second semiconductor regions 5 (see figure 3) of the first conductivity type;

a gate wiring 10 which is formed on the semiconductor layer via a first insulating film 4;

a plurality of main electrodes 14 (see figure 2) which are electrically connected to the plurality of second semiconductor regions and which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes, and upper surfaces of the main electrodes 14 are higher than an upper surface of the gate wiring.

Narazaki et al. do not teach a connecting plate which is directly connected onto the upper surfaces of the main electrodes.

AAPA teaches in figure 21 a connecting plate is directly connected onto the upper surfaces of the main electrodes of the device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a connecting plate directly onto the upper surfaces of the electrodes of Narazaki et al.'s device in order to provide good connection between the source electrodes and the external wirings.

Regarding claims 4, 21-23 and 39-41, AAPA teaches gate wiring 2107 comprising aluminum, and a connecting plate connected to a lead frame. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form

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the main electrodes and the connecting plate of a plurality of metal layers comprising aluminum and to connect the connecting plate to a lead frame in Narazaki et al.'s device in order to reduce the contact resistance between the main electrodes and the lead frame and in order to provide external connections to the device.

Regarding claim 4, Narazaki et al. teach a second insulating film extends between plurality of metal layers.

Regarding claim 5, Narazaki et al. teach in figure 1 plurality of main electrodes are formed apart from the gate wiring with a gap there between.

Regarding the process limitations recited in claims 23 and 41 ("the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding") these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious

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product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 6 and 24, Narazaki et al. teach a first gate electrode 7 (see figure 5) which is formed in the cell forming region and controls continuity between the first semiconductor region and the second semiconductor region; and a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions respectively and which are formed at predetermined intervals in the cell forming region on the semiconductor layer.

Regarding claim 24, Narazaki et al. teach a second semiconductor layer 3 of a second conductivity type which is formed on the first semiconductor layer 2; first and second semiconductor regions 5 (see figure 3) of the first conductivity type which is formed in first and second cell forming regions in the second semiconductor layer.

### ***Response to Arguments***

Applicant argues that Narazaki et al. do not teach upper surfaces of the main electrodes are higher than an upper surface of the gate wiring, because the upper surfaces of the main electrodes 14 are at the same level as the upper surface of the gate wiring 13.

Although the upper surfaces of the main electrodes 14 are at the same level as the majority of the upper surfaces of the gate wiring 13, an upper surface of the gate wiring at the middle of the gate wiring 13 (located above region 5) is lower than the upper surfaces of the main electrodes 14. Therefore, Narazaki et al. teach upper surfaces of the main electrodes are higher than an upper surface of the gate wiring, as claimed.

Applicant argues that connecting a connecting plate onto the upper surfaces of the main electrodes of Narazaki et al. would short circuit the main electrodes to the gate wiring.

Applicant hypothesizes that connecting a connecting plate onto the upper surfaces of the main electrodes of Narazaki et al. would short circuit the main electrodes to the gate wiring. Short circuiting the main electrodes to the gate wiring would render the device inoperable. Clearly, an artisan forming Narazaki et al.'s device would not form an inoperable device by short circuiting the main electrodes to the gate wiring.

### **Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.



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Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized, cursive script.

O.N.  
4/10/05

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800